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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Joseph E. Geusic et al.

Title: INTEGRATED CIRCUITS USING OPTICAL FIBER INTERCONNECTS FORMED THROUGH A SEMICONDUCTOR WAFER AND METHODS FOR FORMING SAME

Attorney Docket No.: 303.390US3

PATENT APPLICATION TRANSMITTAL

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X **CONTINUATION** of prior Patent Application No. 09/031,975 (under 37 CFR § 1.53(b)) comprising:
- X Specification (20 pgs, including claims numbered 1 through 38 and a 1 page Abstract).
- X Formal Drawing(s) (4 sheets).
- X Copy of signed Declaration (9 pgs) from prior application.
- X Copy of Power of Attorney from prior application (1 pg.)
- X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
- X Check in the amount of $690.00 to pay the filing fee.

X Prior application is assigned of record to Micron Technology, Inc..
X Information Disclosure Statement (1 pgs), Form 1449 (4 pgs). References NOT enclosed, cited in prior application.
X Preliminary Amendment (1 pgs).

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Integrated Circuits Using Optical Fiber Interconnects Formed Through a Semiconductor Wafer and Methods for Forming Same

Technical Field of the Invention

The present invention relates generally to the field of integrated circuits and, in particular, to integrated circuits using optical fiber interconnects formed through a semiconductor wafer and methods for forming same.

Background of the Invention

Electrical systems typically use a number of integrated circuits that are mounted on a printed circuit board. The individual integrated circuits of the system are typically fabricated on different wafers. Each wafer is tested and separated into individual dies or chips. Individual chips are then packaged as individual integrated circuits. Each integrated circuit includes a number of leads that extend from the packaging of the circuit. The leads of the various integrated circuits, are interconnected to allow information and control signals to be passed between the integrated circuits such that the system performs a desired function. For example, a personal computer includes a wide variety of integrated circuits, e.g., a microprocessor and memory chips, that are interconnected on one or more printed circuit boards in the computer.

While printed circuit boards are useful for bringing together separately fabricated and assembled integrated circuits, the use of printed circuit boards creates some problems which are not so easily overcome. For example, printed circuit boards consume a large amount of physical space compared to the circuitry of the integrated circuits which are mounted to them. It is desirable to reduce the amount of physical space required by such printed circuit boards. Further, assuring the electrical integrity of interconnections between integrated circuits mounted on a printed circuit board is a challenge. Moreover, in certain applications, it is desirable to reduce the physical length

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Applicant:	Joseph E. Geusic et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.390US3
Title:	INTEGRATED CIRCUITS USING OPTICAL FIBER INTERCONNECTS FORMED THROUGH A SEMICONDUCTOR WAFER AND METHODS FOR FORMING SAME	

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Before taking up the above identified application for Examination, please enter the following amendment.

IN THE SPECIFICATION

On page 1, line 6, before "The present invention", please insert the following --This application is a Continuation of U.S. application, Serial No. 09/031,975, filed on February 26, 1998.--

IN THE CLAIMS

Please cancel claims 2-38 without prejudice or disclaimer.

CONCLUSION

Claims 2-38 are canceled. Claim 1 is now pending in the application. Applicant will file additional claims in a Supplemental Preliminary Amendment. If the Examiner begins the examination without receiving the new claims, it is respectfully requested that the Examiner contact the below signed attorney to receive a copy of the new claims.

Respectfully submitted,

JOSEPH E. GEUSIC ET AL.

By their Representatives,

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of electrical interconnections between devices because of concerns with signal loss or dissipation and interference with and by other integrated circuitry devices.

A continuing challenge in the semiconductor industry is to find new, innovative, and efficient ways of forming electrical connections with and between circuit devices which are fabricated on the same and on different wafers or dies. Relatedly, continuing challenges are posed to find and/or improve upon the packaging techniques utilized to package integrated circuitry devices. As device dimensions continue to shrink, these challenges become even more important.

For reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for an improved technique for interconnecting individual integrated circuits in an electronic system.

Summary of the Invention

The above mentioned problems with integrated circuits and other problems are addressed by the present invention and will be understood by reading and studying the following specification. Integrated circuits are described which use optical fibers that extend through the thickness of a semiconductor substrate or wafer so as to allow communication between integrated circuits formed on opposite sides of a single wafer, on opposite sides of two wafers that are bonded together, formed on wafers in a stack that are bonded together, or other appropriate configuration of wafers.

In one embodiment, a method for interconnecting first and second integrated circuits is provided. The first integrated circuit is formed on a working surface of a first semiconductor substrate. At least one high aspect ratio hole is formed through the first semiconductor substrate. An optical fiber with a cladding layer and a core is formed in the at least one high aspect ratio hole. The optical fiber having first and second ends. The first integrated circuit is coupled to the second integrated circuit through the optical fiber. In one embodiment, the second integrated circuit is formed on a second surface of the first semiconductor substrate, opposite the working surface of the first

semiconductor substrate. In another embodiment, the second integrated circuit is formed on a working surface of a second semiconductor substrate. The second semiconductor substrate is bonded to the first semiconductor substrate such that the first and second integrated circuits are coupled together through the optical fiber in the first semiconductor substrate. In another embodiment, the surfaces of the first and second semiconductor substrates that are bonded together are located on sides of the first and second semiconductor substrates that are opposite the working surfaces of the first and second semiconductor substrates, respectively.

In another embodiment, an electronic system is provided. The electronic system includes at least one semiconductor wafer. A number of integrated circuits are also provided. At least one integrated circuit is formed on the at least one semiconductor wafer. The at least one semiconductor wafer includes at least one optical fiber formed in a high aspect ratio hole that extends through the thickness of the at least one semiconductor wafer. At least one optical transmitter and at least one optical receiver are associated with the at least one optical fiber. The optical transmitter and optical receiver transmit optical signals between selected integrated circuits of the electronic system over the optical fiber.

In another embodiment, an integrated circuit is provided. The integrated circuit includes a functional circuit formed on a wafer. A number of optical fibers are formed in high aspect ratio holes that extend through the wafer. The optical fibers include a cladding layer and a center core that are formed from materials with different indices of refraction.

In another embodiment, a method for forming an integrated circuit in a semiconductor wafer with an optical fiber that extends through the semiconductor wafer is provided. The method includes forming a functional circuit in a first surface of the semiconductor wafer. A number of etch pits are formed in the first surface of the semiconductor wafer at selected locations in the functional circuit An anodic etch of the semiconductor wafer is performed such that high aspect ratio holes are formed through the semiconductor wafer from the first surface to a second, opposite surface. A

cladding layer of an optical fiber is formed on an inner surface of the high aspect ratio holes. A core layer of the optical fiber is also formed. The optical fiber is selectively coupled to the functional circuit.

In another embodiment, a method for forming an optical fiber through a semiconductor substrate is provided. The method includes forming at least one high aspect ratio hole through the semiconductor substrate that passes through the semiconductor substrate from a first working surface to a surface opposite the first working surface. A cladding layer of an optical fiber is formed on an inner surface of the at least one high aspect ratio hole. A core layer of the optical fiber is also formed. In one embodiment, the cladding layer comprises an oxide layer formed in the high aspect ratio holes. In another embodiment, the core layer comprises a layer of an oxide with an index of refraction that is greater than the index of refraction of the cladding layer. In another embodiment, the core layer comprises a layer with a hole that extends substantially along the length of the optical fiber with a diameter that is less than 0.59 times the wavelength of light used to transmit signals over the optical fiber.

Brief Description of the Drawings

Figures 1A, 1B, and 1C are elevational views of exemplary embodiments of an integrated circuit with a semiconductor wafer having an optical fiber formed in an high aspect ratio hole that extends through the semiconductor wafer according to the teachings of the present invention.

Figure 2, 3, 4, 5, 6, and 7 are views of a semiconductor wafer at various points of an illustrative embodiment of a method for forming an integrated circuit with optical fibers formed through at least one semiconductor wafer according to the teachings of the present invention.

Figures 8 and 9 are graphs that show guided waves in optical fibers according to the teachings of the present invention.

Detailed Description

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific illustrative embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

In the following description, the terms wafer and substrate are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizonal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

Figure 1A is an elevational view of an embodiment of the present invention. Electronic system 105a includes semiconductor wafer 100a. Semiconductor wafer 100a includes at least one optical fiber 102a that provides a path for transmitting signals between functional circuit 108a on a first surface of semiconductor wafer 100a and functional circuit 109a on a second, opposite surface of semiconductor wafer 100a. It is noted that a number of optical fibers can be formed through semiconductor wafer 100a.

Optical fiber 102a is formed in a high aspect ratio hole in semiconductor wafer 100a. The high aspect ratio hole is formed using, for example, an anodic etching technique as described in more detail below. Typically, the high aspect ratio holes have an aspect ratio in the range of approximately 100 to 200. Conventionally, a semiconductor wafer has a thickness in the range of approximately 100 to 1000 microns. Thus, the high aspect ratio holes used to form the optical fibers can be fabricated with a width that is in the range from approximately 0.5 microns to approximately 10 microns.

Optical fiber 102a is coupled to functional circuits 108a and 109a. For example, optical transmitter 104a is coupled to one end of optical fiber 102a and optical receiver 106a is coupled to a second, opposite end of optical fiber 102a. Optical transmitter 104a is also coupled to a node of functional circuit 108a and optical receiver 106a is coupled to a node of functional circuit 109a. In one embodiment, optical transmitter 104a comprises a gallium arsenide transmitter that is bonded to the first surface of semiconductor wafer 100a using conventional wafer bonding techniques. In this embodiment, optical receiver 106a comprises a silicon photodiode detector formed in the second surface of semiconductor wafer 100a. In other embodiments, other appropriate optical receivers and transmitters may be used to transmit signals over optical fiber 102a.

Optical fiber 102a comprises cladding layer 112a that separates core 110a from semiconductor wafer 100a. In this structure, semiconductor wafer 100a acts as the outer "sheath" for optical fiber 102a. Various materials can be used to form core 110a and cladding layer 112a. Basically, core 110a comprise a material with a higher index of refraction than the material of cladding layer 112a and thus provides normal optical fiber waveguide characteristics. Specific examples of materials for core 110a and cladding layer 112a are provided below with respect to Figures 6 and 7.

Since the optical fiber is formed in a wafer of semiconductor material, absorption by and radiation in the semiconductor wafer can affect the operation of the optical fiber. For example, if the wavelength of the light transmitted in optical fiber

102a is greater than the absorption edge of the semiconductor wafer, e.g., 1.1 microns for silicon, then semiconductor wafer 100a will not absorb the light transmitted in optical fiber 102a. However, due to the large change in index of refraction at the interface between cladding layer 112a and semiconductor wafer 100a, some radiation loss occurs into semiconductor wafer 100a. This case is depicted, for example, in Figure 8.

Figure 8 is a graph that illustrates the magnitude of the radiation in optical fiber 102a along a diameter of optical fiber 102a. In the region of core 256, indicated at 801, optical waves are guided with no substantial loss along the length of optical fiber 102a. Evanescent fields are present in the region of cladding layer 254 as indicated at 802. These evanescent fields drop off to insignificant levels as indicated at 800 in the surrounding semiconductor wafer.

In the case of shorter wavelength light transmitted in optical fiber 102a, there will be some absorption as well as radiation into the semiconductor substrate. For example, with a silicon wafer, light with a wavelength of less than 1.1 microns produces some small losses due to absorption and radiation into the silicon wafer.

In some cases, it is advantageous to limit the penetration of the optical wave into semiconductor wafer 100a. This avoids problems related to possible photoregeneration of carriers in the surrounding semiconductor wafer 100a that might interfere with the normal operation of other integrated circuitry. To prevent optical waves from penetrating the semiconductor wafer, the hole that houses the optical fiber can be lined with a reflecting metal mirror prior to forming the cladding layer. A technique for forming the metal layer is described in co-pending application, Serial No. ____, entitled *Integrated Circuits Using Optical Waveguide Interconnects Formed Through a Semiconductor Wafer and Methods for Forming Same*, (attorney docket no. 303.382US1), which application is incorporated by reference.

Optical fibers can be added to circuits using a conventional layout for the circuit without adversely affecting the surface area requirements of the circuit. Conventional circuits typically include pads formed on the top surface of the semiconductor wafer that

are used to connect to leads of the integrated circuit through bonding wires. Advantageously, the bonding wires of conventional circuits can be replaced by optical fibers 102a to allow signals to be passed between various integrated circuits of electronic system 105a without the need to attach the individual integrated circuits to a printed circuit board. This allows a substantial space savings in the design of electrical systems along with overcoming concerns related to signal loss or dissipation and interference with and by other integrated circuitry devices in the electrical system.

Figures 1B and 1C show additional embodiments of electronic systems using optical fibers formed through integrated circuits to interconnect various integrated circuits. In the embodiment of Figure 1B, integrated circuits 108b and 109b are formed in working surfaces of semiconductor wafers 100b and 101b. Surfaces opposite the working surfaces of semiconductor wafers 100b and 101b are bonded together using conventional wafer bonding techniques. Optical fiber 102b transmits signals between integrated circuits 108b and 109b. A portion of optical fiber 102b is formed in each of the semiconductor wafers 100b and 101b. In the embodiment of Figure 1C, semiconductor wafers 100c and 101c are stacked with the working surface of semiconductor wafer 101c beneath the surface of semiconductor wafer 100c that is opposite the working surface of semiconductor wafer 100c. In this embodiment, optical fiber 102c is formed within semiconductor wafer 100c.

Figure 2, 3, 4, 5, 6, and 7 are views of semiconductor wafer 200 at various points of an illustrative embodiment of a method for forming optical fibers through a semiconductor wafer according to the teachings of the present invention. Functional circuit 202 is formed in an active region of semiconductor wafer 200. For purposes of clarity, the Figures only show the formation of two optical fibers through semiconductor wafer 200. However, it is understood that with a particular functional circuit any appropriate number of optical fibers can be formed. Essentially, the optical fibers are formed in the same space on the surface of semiconductor wafer 200 that is conventionally used to form bonding pads for leads. In a conventional circuit, the leads of the integrated circuit are connected to a printed circuit board which routes signals to

other integrated circuits. The optical fibers advantageously remove the need for a printed circuit board to interconnect the functional circuits formed on individual semiconductor wafers.

As shown in Figure 2, photo resist layer 204 is formed on surface 206 of semiconductor substrate 200. Photo resist layer 204 is patterned to provide openings 208 at points on surface 206 where high aspect ratio holes are to be formed through semiconductor wafer 200.

As shown in Figure 3, etch pits 210 are formed by standard alkaline etching through openings 208 in photo resist layer 204. Photo resist layer 204 is then removed.

Figure 4 is a schematic diagram that illustrates an embodiment of a layout of equipment used to carry out an anodic etch that is used to form high aspect ratio holes 250 of Figure 5. Typically, holes 250 have an aspect ratio in the range of 100 to 200. Bottom surface 262 of semiconductor wafer 200 is coupled to voltage source 234 by positive electrode 230. Further, negative electrode 232 is coupled to voltage source 234 and is placed in a bath of 6% aqueous solution of hydrofluoric acid (HF) on surface 206 of semiconductor wafer 200.

In this example, illumination equipment 236 is also included because semiconductor wafer 200 is n-type semiconductor material. When p-type semiconductor material is used, the illumination equipment is not required. Illumination equipment 236 assures that there is a sufficient concentration of holes in semiconductor wafer 200 as required by the anodic etching process. Illumination equipment 236 includes lamp 238, IR filter 240, and lens 242. Illumination equipment 236 focuses light on surface 262 of semiconductor wafer 200.

In operation, the anodic etch etches high aspect ratio holes through semiconductor wafer 200 at the location of etch pits 210. Voltage source 234 is turned on and provides a voltage across positive and negative electrodes 230 and 232. Etching current flows from surface 206 to positive electrode 230. This current forms the high aspect ratio holes through semiconductor wafer 200. Further, illumination equipment illuminates surface 262 of semiconductor wafer 200 so as to assure a sufficient

concentration of holes for the anodic etching process. The size and shape of the high aspect ratio holes through semiconductor wafer 200 depends on, for example, the anodization parameters such as HF concentration, current density, and light illumination. An anodic etching process is described in V. Lehmann, *The Physics of Macropore Formation in Low Doped n-Type Silicon,* J. Electrochem. Soc., Vol. 140, No. 10, pp. 2836-2843, Oct. 1993, which is incorporated herein by reference.

As shown in Figure 5, cladding layer 254 is formed on surface 252 of high aspect ratio holes 250. Further, core 256 is formed within hole 250 such that cladding layer 254 and core 256 comprise optical fiber 258.

Core 256 has an index of refraction that is greater than the index of refraction of cladding layer 254. Cladding layer 254 may comprise, for example, a transparent dielectric film such as silicon oxide (SiO_2), aluminum oxide (Al_2O_3), a nitride, other oxide, or other appropriate dielectric material. Cladding layer 254 is deposited with a uniformity that allows light to be transmitted through optical fiber 258 with normal optical fiber waveguide characteristics. When a nitride is used, cladding layer 254 can be deposited with the required uniformity using the technique described in K.P. Muller, et al, *Trench Node Technology for Gigabit DRAM Generations,* 1996 IEDM Technical Digest, p. 507-510 which is incorporated by reference. This technique allows nitride films to be deposited at low temperatures and low deposition rates to insure uniform coverage of very deep trenches. A technique referred to as "atomic layer epitaxy" can also be used to deposit cladding layer 254. Atomic layer epitaxy has been described for use with the deposition of silicon oxide (SiO_2), *See* J. W. Klaus, et al, *Atomic Layer Controlled Growth of SiO_2 Films Using Binary Reaction Sequence Chemistry,* Appl. Phys. Lett. 70(9), 3 March 1997, pp. 1092-1094, which is incorporated by reference. Further, atomic layer epitaxy has been described for use with deposition of aluminum oxide (Al_2O_3). The atomic layer epitaxy technique deposits material with a thickness of 1 to 2 angstroms for a single binary reaction sequence. Thus, the technique advantageously allows the high aspect ratio holes that house the optical fibers to be lined with a uniform cladding layer.

In one embodiment, optical fiber 258 transmits light with a wavelength that is greater than 1.1 microns. In this embodiment, cladding layer 254 comprises silicon oxide (SiO_2) with an index of refraction of approximately 1.5 or aluminum oxide (Al_2O_3) with an index of refraction of approximately 1.7. Core 256 comprises lightly doped polysilicon. The lightly doped polysilicon has an index of refraction of approximately 3.4 and exhibits low optical absorption at wavelengths of greater than 1.1 microns. Optical fiber 258 of this embodiment is shown in cross section in Figure 6.

In another embodiment, cladding layer 254 comprises silicon oxide (SiO_2) and core 256 comprises an oxide or nitride with a higher index of refraction, e.g., aluminum oxide (Al_2O_3). A cross section of optical fiber 258 of this embodiment is shown in Figure 7. Core 256 does not completely fill the center of optical fiber 258. Hole 262 extends along the length of core 256 through semiconductor wafer 200. However, as long as hole 262 has a diameter that is less than 0.59 times the wavelength of the light transmitted over optical fiber 258, the light will still be guided by core 256 as shown in Figure 9.This embodiment can transport light with a wavelength that is less than 1.1 microns. This allows a gallium arsenide emitter to be used at one end of optical fiber 258 to transmit signals down optical fiber 258 and a simple silicon photodiode detector to be used as the receiver on the opposite end of optical fiber 258.

Figure 9 is a graph that illustrates the magnitude of the radiation in an optical fiber of the type shown in Figure 7 along a diameter of the optical fiber. In the region of hole 262, an evanescent field is present as indicated at 900. In the region of core 256, radiation in the optical fiber is guided along the length of the fiber without significant loss in intensity. Evanescent fields are present in the region of cladding layer 254 as indicated at 904. These evanescent fields drop off to insignificant levels as indicated at 906 in the surrounding semiconductor wafer.

Conclusion

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is

calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, other materials such as oxides, nitrides, or high index glasses can be used to form the cladding layer and the core of an optical fiber that extends through a semiconductor wafer. It is noted that optical fibers 102 and 258 can transmit signals in either direction through the semiconductor wafer by proper placement of transmitters and receivers. Further, electronic systems can include more than two semiconductor wafers with sufficient optical fibers formed through the semiconductor wafers to allow signals to be communicated between the integrated circuits of the various semiconductor wafers.

Advantageously, using optical fibers according to the teachings of the present invention allows electronic systems to be constructed in less physical space compared to conventional electronic systems by removing the need for large printed circuit boards to interconnect various integrated circuits. This also provides the advantage of reducing the cost of packaging integrated circuits for a particular electronic system by allowing a number of circuits to be packaged together. Further, using the optical fibers assures the electrical integrity of interconnections between integrated circuits by reducing the physical length of electrical interconnections between devices. This reduces concerns with signal loss or dissipation and interference with and by other integrated circuitry devices.

What is claimed is:

1. A method for interconnecting first and second integrated circuits, wherein the first integrated circuit is formed on a working surface of a first semiconductor substrate, the method comprising:

forming at least one high aspect ratio hole through the first semiconductor substrate;

forming an optical fiber with a cladding layer and a core in the at least one high aspect ratio hole, the optical fiber having first and second ends; and

coupling the first integrated circuit to the second integrated circuit through the optical fiber.

2. The method of claim 1, and further comprising forming the second integrated circuit on a second surface, opposite the working surface of the first semiconductor substrate.

3. The method of claim 1, and further comprising:

forming the second integrated circuit in a working surface of a second semiconductor substrate; and

bonding the first and second semiconductor substrates together such that the first and second integrated circuits are coupled together through the optical fiber in the first semiconductor substrate.

4. The method of claim 3, wherein bonding the first and second semiconductor substrates together comprises bonding surfaces of the first and second semiconductor substrates that are opposite the working surfaces of the first and second semiconductor substrates.

5. The method of claim 3, wherein bonding the first and second semiconductor substrates together comprises bonding a working surface of the second semiconductor

substrate with a surface of the first semiconductor substrate that is opposite the working surface of the first semiconductor substrate.

6. The method of claim 1, wherein forming at least one high aspect ratio hole comprises:

forming etch pits at selected locations in the first surface of the semiconductor substrate; and

performing an anodic etch of the first semiconductor substrate such that high aspect ratio holes are formed through the first semiconductor substrate at the location of the etch pits.

7. The method of claim 1, wherein coupling the first integrated circuit to the second integrated circuit comprises forming optical transmitters and receivers on opposite ends of the optical fiber so as to transmit signals between the first and second integrated circuits.

8. The method of claim 7, wherein forming an optical transmitter comprises forming a gallium arsenide optical transmitter that is bonded to a surface of the first semiconductor substrate and forming an optical receiver comprises forming a silicon photodiode detector at an opposite end of the optical fiber.

9. The method of claim 1, wherein forming the optical fiber comprises forming a cladding layer of SiO_2 and forming a core of polysilicon.

10. The method of claim 1, wherein forming the optical fiber comprises forming a cladding layer of Al_2O_3 and forming a core of polysilicon.

11. The method of claim 1, wherein forming the optical fiber comprises forming a cladding layer of SiO_2 and forming a core of Al_2O_3.

12. The method of claim 1, wherein forming the optical fiber comprises forming a core with a hole that runs substantially along the center of the optical fiber wherein the hole has a diameter that is less than 0.59 times the wavelength of the light to be transmitted in the optical fiber.

13. The method of claim 1, wherein forming the optical fiber comprises forming a cladding layer that surrounds a core layer, wherein the core layer has an index of refraction that is greater than the index of refraction of the cladding layer.

14. The method of claim 1, wherein forming the optical fiber comprises forming the cladding layer using atomic layer epitaxy.

15. An electronic system, comprising:

at least one semiconductor wafer;

a number of integrated circuits with at least one integrated circuit formed on the at least one semiconductor wafer;

the at least one semiconductor wafer including at least one optical fiber formed in a high aspect ratio hole that extends through the thickness of the at least one semiconductor wafer; and

at least one optical transmitter and at least one optical receiver associated with the at least one optical fiber that transmit optical signals between selected integrated circuits of the electronic system.

16. The electronic system of claim 15, wherein the number of integrated circuits includes a microprocessor and a memory device.

17. The electronic system of claim 15, wherein the number of optical fibers comprise optical fibers that are formed by an anodic etch that creates high aspect ratio holes through the semiconductor wafer that are filled with a cladding layer and a core.

18. The electronic system of claim 15, wherein each optical fiber comprises a cladding layer of SiO_2 and a core of polysilicon.

19. The electronic system of claim 15, wherein each optical fiber comprises a cladding layer of Al_2O_3 and a core of polysilicon.

20. The electronic system of claim 15, wherein each optical fiber comprises a cladding layer of SiO_2 and a core of Al_2O_3.

21. The electronic system of claim 15, wherein each optical fiber comprises a core with a hole that runs substantially along the center of the optical fiber wherein the hole has a diameter that is less than 0.59 times the wavelength of the light to be transmitted in the optical fiber.

22. The electronic system of claim 15, wherein each optical transmitter comprises a gallium arsenide transmitter and each optical receiver comprises a silicon photodiode detector.

23. The electronic system of claim 15, wherein each optical fiber comprises a cladding layer that surrounds a core layer, wherein the core layer has an index of refraction that is greater than the index of refraction of the cladding layer.

24. An integrated circuit, comprising:

a functional circuit formed on a wafer;

a number of optical fibers formed in high aspect ratio holes that extend through the wafer; and

wherein the optical fibers include a cladding layer and a center core that are formed from materials with different indices of refraction.

25. The integrated circuit of claim 24, wherein the number of optical fibers comprise optical fibers that are formed by an anodic etch that creates high aspect ratio holes through the semiconductor wafer that are filled with a cladding layer and a core.

26. The integrated circuit of claim 24, wherein each optical fiber comprises a cladding layer of SiO_2 and a core of doped polysilicon.

27. The integrated circuit of claim 24, wherein each optical fiber comprises a cladding layer of Al_2O_3 and a core of polysilicon.

28. The integrated circuit of claim 24, wherein each optical fiber comprises a cladding layer of SiO_2 and a core of Al_2O_3.

29. The integrated circuit of claim 24, wherein each optical fiber comprises a core with a hole that runs substantially along the center of the optical fiber but that has a diameter that is less than 0.59 times the wavelength of the light to be transmitted in the optical fiber.

30. The integrated circuit of claim 24, wherein the optical fiber comprises a cladding layer that surrounds a core layer, wherein the core layer has an index of refraction that is greater than the index of refraction of the cladding layer.

31. A method for forming an integrated circuit in a semiconductor wafer with an optical fiber that extends through the semiconductor wafer, the method comprising:

forming a functional circuit in a first surface of the semiconductor wafer;

forming a number of etch pits in the first surface of the semiconductor wafer at selected locations in the functional circuit;

performing an anodic etch of the semiconductor wafer such that high aspect ratio holes are formed through the semiconductor wafer from the first surface to a second, opposite surface;

forming a cladding layer of an optical fiber on an inner surface of the high aspect ratio holes;

forming a core layer of the optical fiber; and

selectively coupling the optical fiber to the functional circuit.

32. The method of claim 31, wherein forming a cladding layer comprises forming an oxide layer in the high aspect ratio holes.

33. The method of claim 31, wherein forming the core layer comprises forming a layer of an oxide with an index of refraction that is greater than the index of refraction of the cladding layer.

34. The method of claim 31, wherein forming the core layer comprises forming a layer with a hole that extends substantially along the length of the optical fiber with a diameter that is less than 0.59 times the wavelength of light used to transmit signals over the optical fiber.

35. A method for forming an optical fiber through a semiconductor substrate, the method comprising:

forming at least one high aspect ratio hole through the semiconductor substrate that passes through the semiconductor substrate from a first working surface to a surface opposite the first working surface;

forming a cladding layer of an optical fiber on an inner surface of the at least one high aspect ratio hole; and

forming a core layer of the optical fiber.

36. The method of claim 35, wherein forming a cladding layer comprises forming an oxide layer in the high aspect ratio holes.

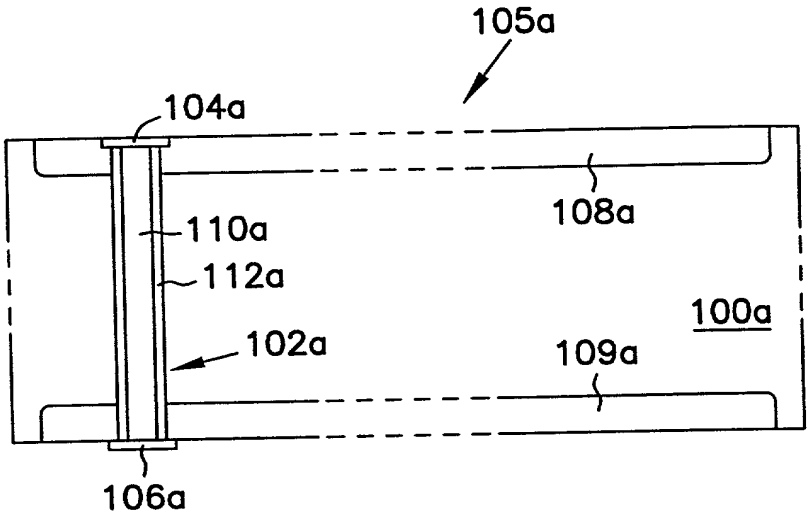
37. The method of claim 35, wherein forming the core layer comprises forming a layer of an oxide with an index of refraction that is greater than the index of refraction of the cladding layer.

38. The method of claim 35, wherein forming the core layer comprises forming a layer with a hole that extends substantially along the length of the optical fiber with a diameter that is less than 0.59 times the wavelength of light used to transmit signals over the optical fiber.

Abstract of the Disclosure

An integrated circuit with a number of optical fibers that are formed in high aspect ratio holes. The high aspect ratio holes extend through a semiconductor wafer. The optical fibers include a cladding layer and a core formed in the high aspect ratio hole. These optical fibers are used to transmit signals between functional circuits on the semiconductor wafer and functional circuits on the back of the wafer or beneath the wafer.

"Express Mail" mailing label number: EL584209491US
Date of Deposit: August 30, 2000
This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.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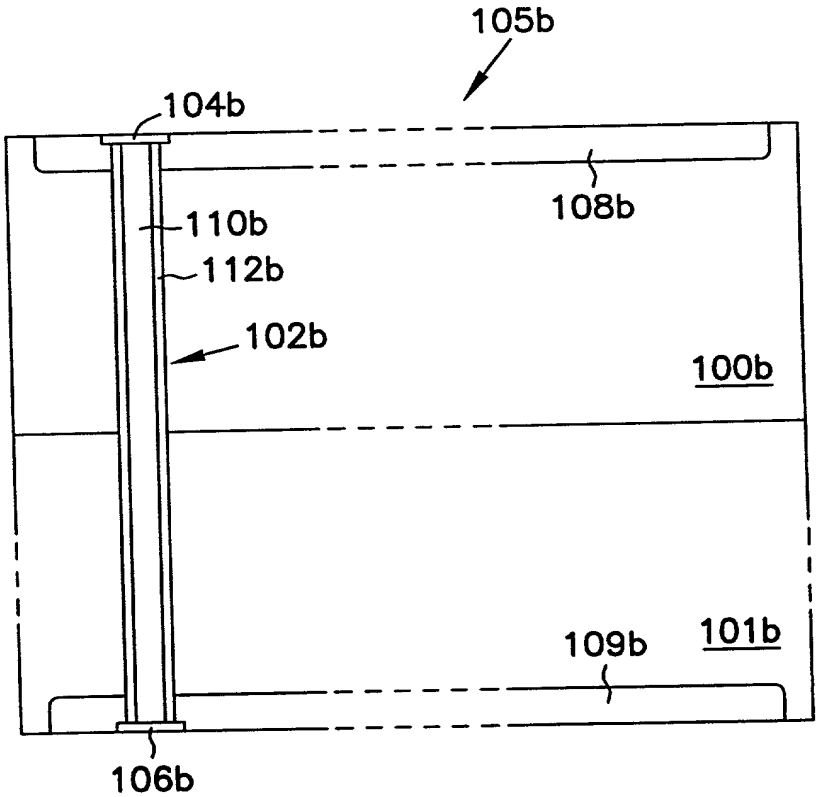
109a
106a

FIG. 1A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106b

FIG. 1B

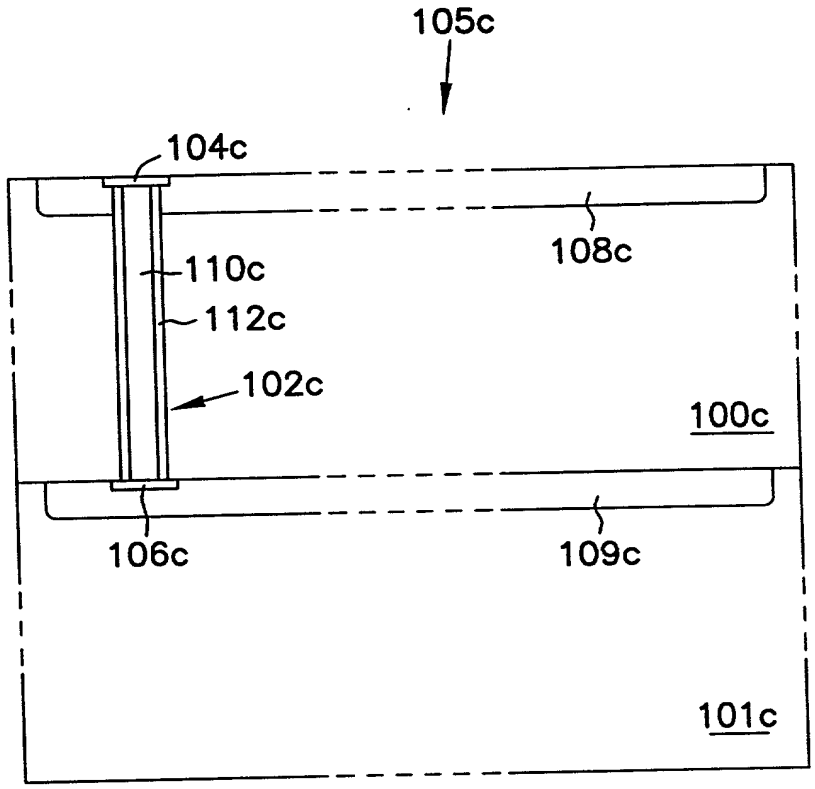


FIG. 1C

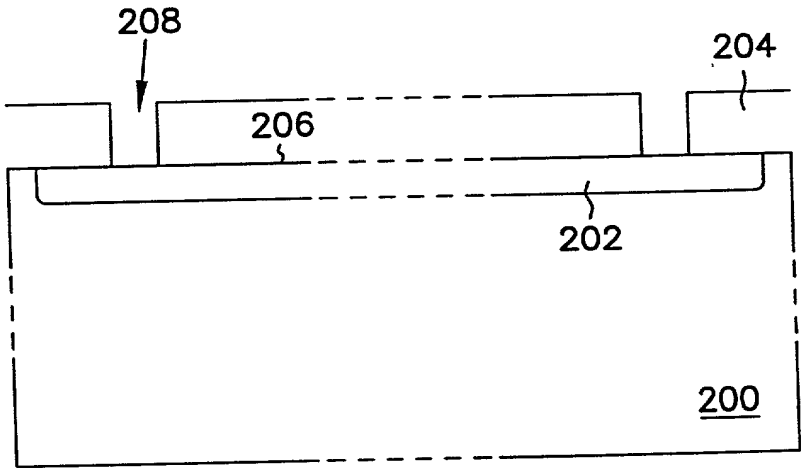


FIG. 2

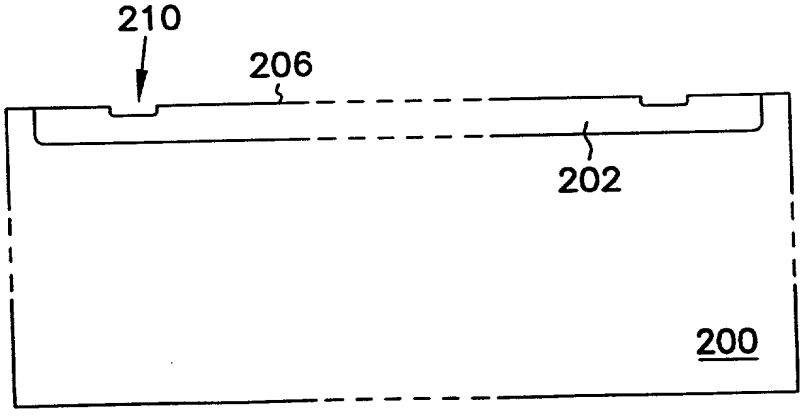
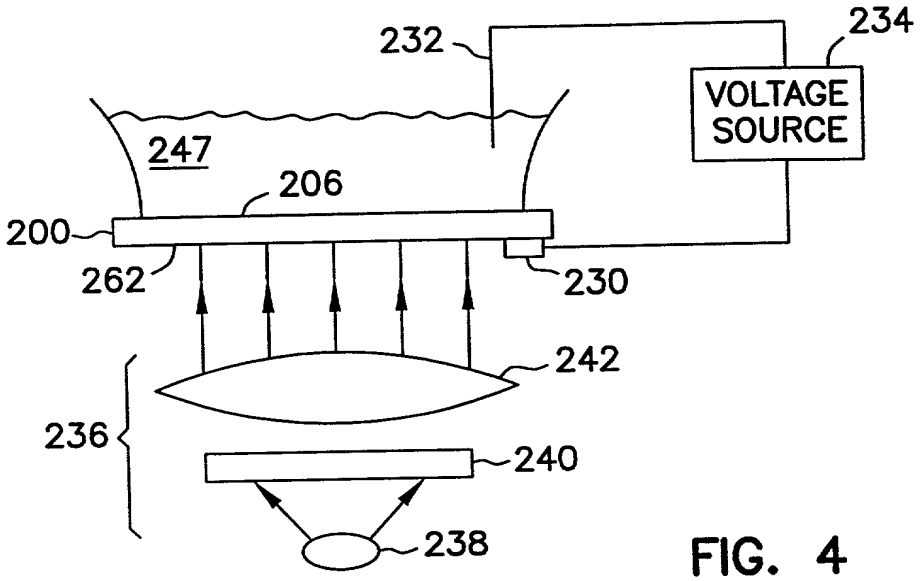


FIG. 3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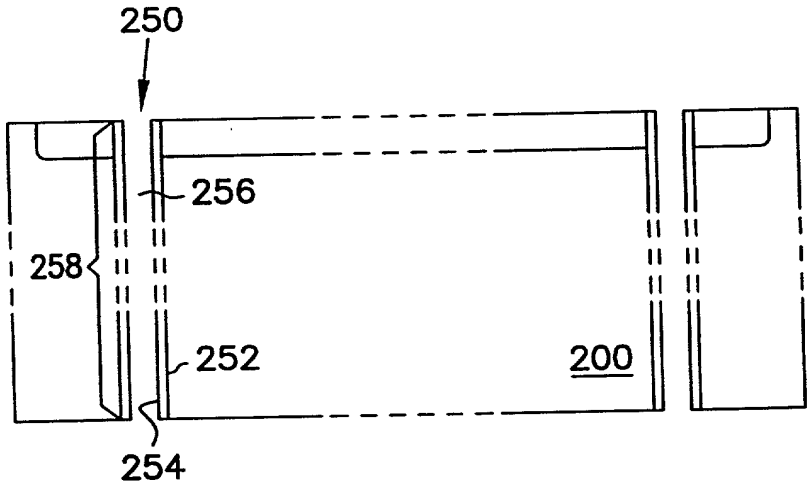
238

FIG. 4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258
252
200
254

FIG. 5

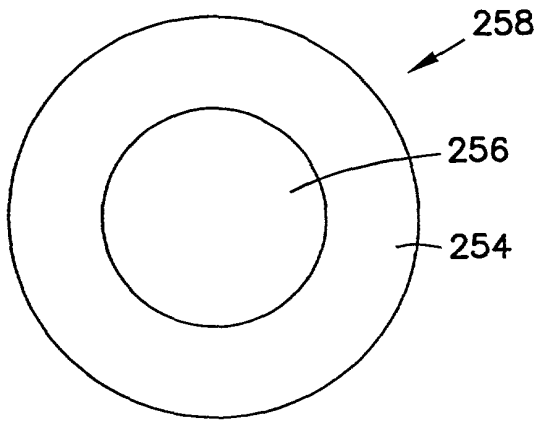

FIG. 6

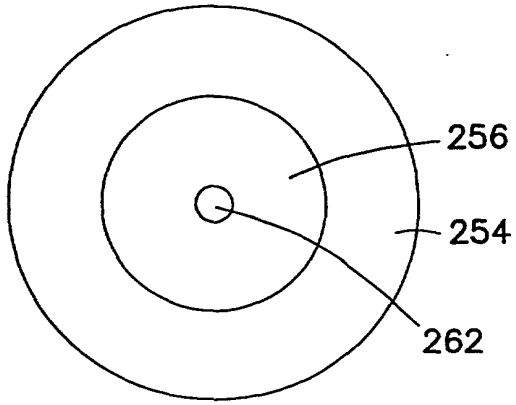

FIG. 7

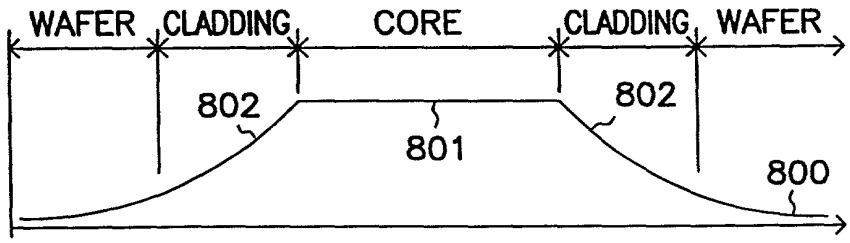

FIG. 8

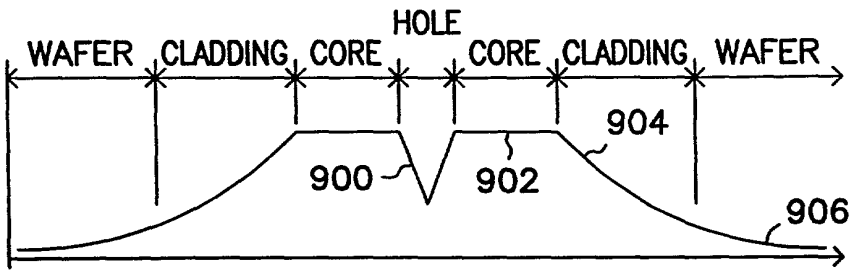

FIG. 9

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

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The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

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I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Joseph E. Geusic**
Citizenship: **United States of America** Residence: **Berkeley Heights, NJ**
Post Office Address: 261 Lorraine Drive
Berkeley Heights, NJ 07922

Signature: Joseph E Geusic Date: 2/17/98
Joseph E. Geusic

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

Full Name of joint inventor number 3 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: _____
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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Signature: _____ Date: _____
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Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: Kie Y. Ahn Date: Feb. 16, 1998
Kie Y. Ahn

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Post Office Address: 965 NW Highland Terrace
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Signature: _____ Date: _____
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Berkeley Heights, NJ 07922

Signature: ______________________ Date: ______________________
Joseph E. Geusic

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Citizenship: **United States of America**
Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: ______________________ Date: ______________________
Kie Y. Ahn

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Citizenship: **United States of America**
Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: ______________________ Date: 18 FEB 98
Leonard Forbes

Full Name of inventor:
Citizenship:
Residence:
Post Office Address:

Signature: ______________________ Date: ______________________

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Signature: _____ Date: 18 FEB 98
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

S/N 09/031,975 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Joseph E. Geusic et al.	Examiner:	
Serial No.:	09/031,975	Group Art Unit:	1104
Filed:	February 26, 1998	Docket:	303.390US1
Title:	INTEGRATED CIRCUITS USING OPTICAL FIBER INTERCONNECTS FORMED THROUGH A SEMICONDUCTOR WAFER AND METHODS FOR FORMING SAME		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Anglin, J. Michael	Reg. No. 24,916	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Arora, Suneel	Reg. No. P-42,267	Forrest, Bradley A.	Reg. No. 30,837	Madrid, Andres N.	Reg. No. 40,710
Bernkopf, Paul A.	Reg. No. P-41,615	Harris, Robert J.	Reg. No. 37,346	McCrackin, Ann M.	Reg. No. P-42,858
Bianchi, Timothy E.	Reg. No. 39,610	Hofmann, Rudolph P., Jr.	Reg. No. 38,187	Provence, David L.	Reg. No. P-43,022
Billion, Richard E.	Reg. No. 32,836	Holloway, Sheryl S.	Reg. No. 37,850	Schwegman, Micheal L.	Reg. No. 25,816
Brennan, Thomas F.	Reg. No. 35,075	Huebsch, Joseph C.	Reg. No. P-42,673	Simboli, Paul B.	Reg. No. 38,616
Brooks, Edward J., III	Reg. No. 40,925	Klima-Silberg, Catherine I.	Reg. No. 40,052	Slifer, Russell D.	Reg. No. 39,838
Clark, Barbara J.	Reg. No. 38,107	Kluth, Daniel J.	Reg. No. 32,146	Taylor, Michael W.	Reg. No. P-43,182
Drake, Eduardo E.	Reg. No. 40,594	Lemaire, Charles A.	Reg. No. 36,198	Viksnins, Ann S.	Reg. No. 37,748
Dryja, Michael A.	Reg. No. 39,662	Litman, Mark A.	Reg. No. 26,390	Woessner, Warren D.	Reg. No. 30,440
Embretson, Janet E.	Reg. No. 39,665				

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Schwegman, Lundberg, Woessner & Kluth, P.A.
Attn: David N. Fogg
P.O. Box 2938
Minneapolis, MN 55402

Telephone: (612) 373-6920
Facsimile: (612) 339-3061

Dated: April 7, 1998

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel